A 2.5 dB Low Noise 6 to 18 GHz HEMT MMIC Amplifier

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ABSTRACT

A 2-stage, 6 to 18 GHz, 15.0 dB gain monolithic GaAs HEMT low noise amplifier was designed, fabricated and tested. A typical noise figure of 2.5 dB and output power of 5 dBm were measured and is believed to be the lowest noise figure reported for a 6 to 18 GHz MMIC Low noise amplifier. This MMIC amplifier exhibits excellent performance at a DC power consumption of 2 volts and 20 mA. This state-of-art performance was achieved using a production 0.25 µm standard HEMT technology without mushroom gates. Low DC power consumption, low noise figure and high gain makes this device well suited for front-end receiver applications.

INTRODUCTION

Broadband phased array systems and EW receivers require low noise front-end amplifiers to achieve good system sensitivity. For the system designer, a low noise 6-18 GHz amplifier with low DC power consumption, small size and high reliability is always subject of interest. With the maturity of GaAs 0.25µm HEMT MMIC technology, it is now possible to design a manufacturable low noise MMIC amplifier that covers the 6-18 GHz band with less than a 3.0 dB noise figure.

This paper describes a monolithic 2-stage, 6-18 GHz reactively matched low noise amplifier designed for the above mentioned applications. The circuit uses two 0.25x150 µm GaAs HEMT devices with series inductive feedback on the front device to achieve a broadband low noise match over the 6-18 frequency band. The typical noise figure of 2.5 dB with associated gain of 15 dB and DC power consumption of 40 mW has made this device an outstanding MMIC for EW applications.

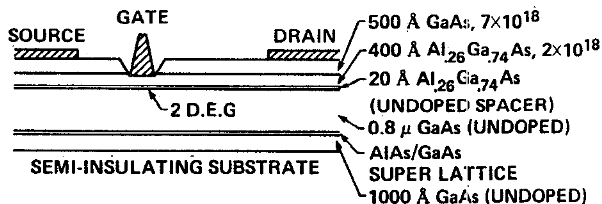

Figure 1. Cross-sectional view of the MBE GaAs HEMT structure

MATERIAL AND DEVICE CHARACTERIZATION

Figure 1 shows a cross-sectional view of the MBE material structure for this standard GaAs HEMT device. This standard GaAs low noise HEMT material structure has been used since 1987 to design several LNAs and consistently produced high performance low noise amplifier up to 20 GHz [1].

A 0.25X150 µm GaAs HEMT test device with the standard gate profile was fabricated on a 100 µm thick GaAs substrate first for device characterization. The test device, shown in Figure 2, was designed for on-wafer probing.

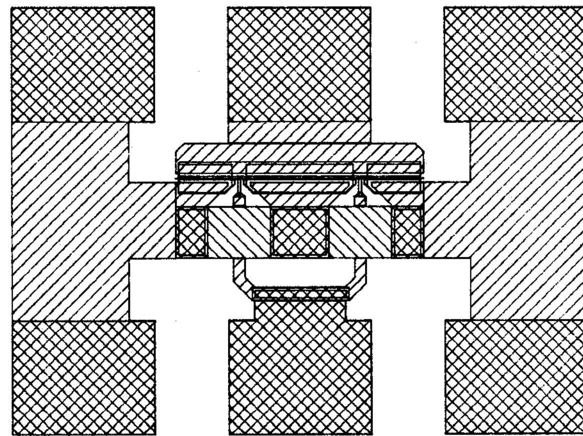

Figure 2. CAD layout of the 0.25x150 µm GaAs HEMT device

I-V characteristics of the HEMT were examined to determine a suitable range of bias conditions for proper operation of the device. In order to design a two-stage amplifier with minimum possible noise figure, both noise

92CH3162-5/92/0000-0021$01.00 © 1992 IEEE

parameters and associated gain were characterized. The trade-offs between minimum device noise figure and the second stage noise contribution were studied. Several bias conditions, V_{ds}=2.0V and I_{ds}=15%,25%,33% and 50% of I_{dss} were selected for the trade-off study. Measured noise and S parameters were obtained using on wafer extraction techniques for each bias point. On wafer extraction of the device parameters greatly reduce the uncertainty of the noise parameters and enhanced the first pass success.

The device model for the 0.25x150 μm HEMT operating at V_{ds}=2.0V and I_{ds}=33%I_{dss} is shown in Figure 3. This device has a F_{min} of 1.26 dB with an associated gain of 8.1 dB at 18 GHz under 33% I_{dss} bias condition and F_{min} of 1.7 dB with associated gain of 9.5 dB at 50% I_{dss} bias condition.

CIRCUIT DESIGN

The principal objective was to design a 3 dB noise figure and 15 dB gain MMIC amplifier that covers the 6 to 18 GHz frequency band. A 2-stage circuit topology was chosen to achieve the targeted specifications. Two 0.25X150 μm HEMTs were used as the first and second stage active devices. Each HEMT was biased at 2.0V and 33% I_{dss}. The 33% I_{dss} bias point was found to provide the optimum noise figure for the two-stage amplifier. Reactive matching was selected because it provided the best broadband noise performance, but due to differences in the required match for noise and input VSWR, series inductive feedback was used to pull the Γ_{opt} and S^*_{11} closer together. The Initial value for the feedback inductor was determined by constructing Fukui's noise circles [2] for three of the frequencies (low,mid,high) and determining the amount of inductance required to transform the noise circles to the desired input match. A practical input matching network was then synthesized from the Smith chart.

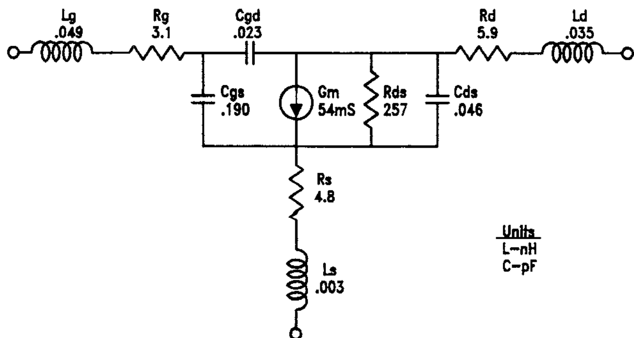

Figure 3. Equivalent circuit model of the 0.25x150 μm HEMT

The inter-stage and output matching networks were synthesized using the methods described by Mellor [3]. A resistive drain network was used for each active device to enhance the amplifier's stability and to compensate for the transistor's inherent gain slope. A schematic of the amplifier is shown in figure 4. The complete amplifier circuit was analyzed using Libra and each of the circuit elements were adjusted to attain the desired performance goals. Figure 5A shows the computer simulated small signal gain, input VSWR and output VSWR. Simulated noise figure is shown in Figure 5B.

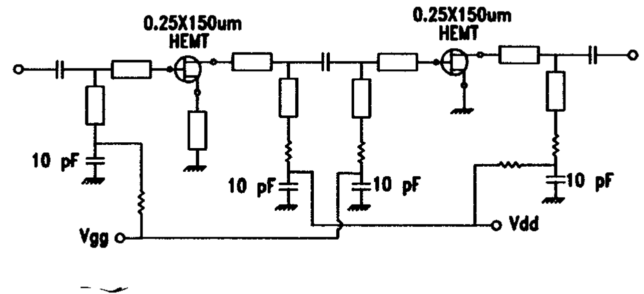

Figure 4. 6-18 GHz LNA circuit Schematic

FABRICATION AND MEASURED RESULTS

The MMIC was fabricated on a 100 μm thick GaAs substrate. A standard low noise AlGaAs HEMT material structure was used. The 0.25 μm gates were defined using E-beam photolithography. This MMIC process features tantalum nitride thin film resistors, silicon nitride dielectric for MIM capacitors and device passivation, plated air-bridges and conductors, via holes were fabricated using reactive ion etching.

The small signal gain, input and output return losses were measured on-wafer using coplanar wafer probes. Figure 6A shows the on-wafer input VSWR and small signal gain measured results. Output VSWR and isolation are shown in Figure 6B. The wafer was then diced and the MMIC chip was assembled in a microstrip test fixture for noise figure and output power measurements. The measured noise figure of this single-ended LNA MMIC is shown in Figure 6C. Noise figures were measured at 25°C with 0.4 dB correction at 18 GHz for the loss of microstrip test fixture. Both small signal gain and noise figure agree well with the computer simulated results.

A photograph of the MMIC LNA chip is shown in Figure 7. The size of the MMIC is 0.064" x 0.064" x 0.004".

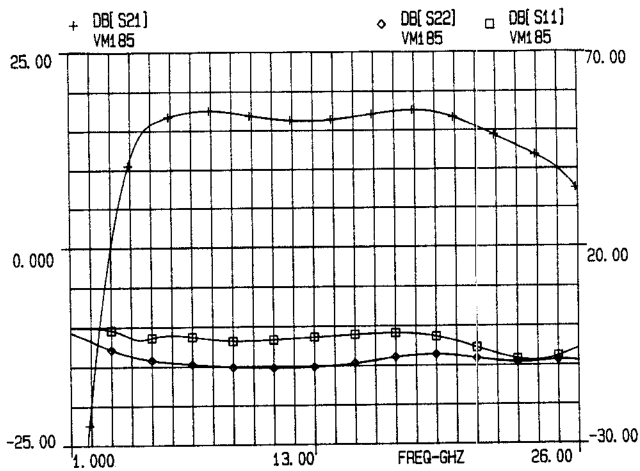

Figure 5A. Computer simulated small signal gain, input and output VSWRs.

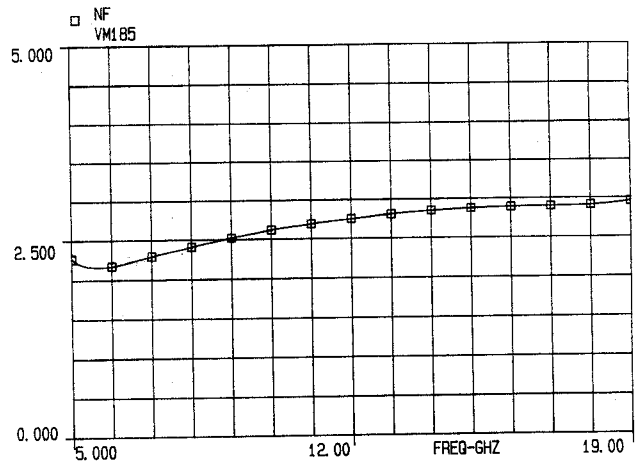

Figure 5B. Computer simulated LNA noise figure

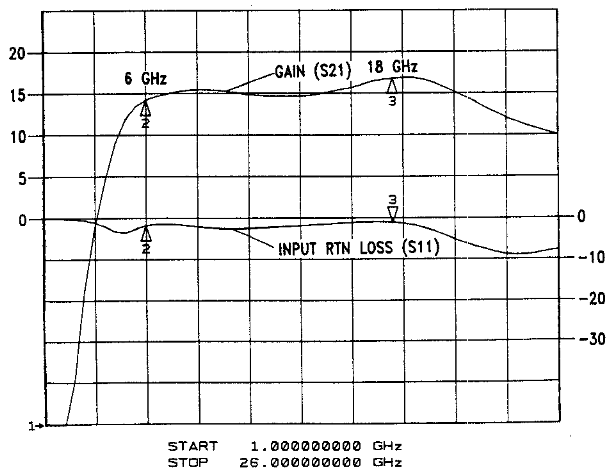

Figure 6A. On-wafer measured LNA small signal gain and input VSWR

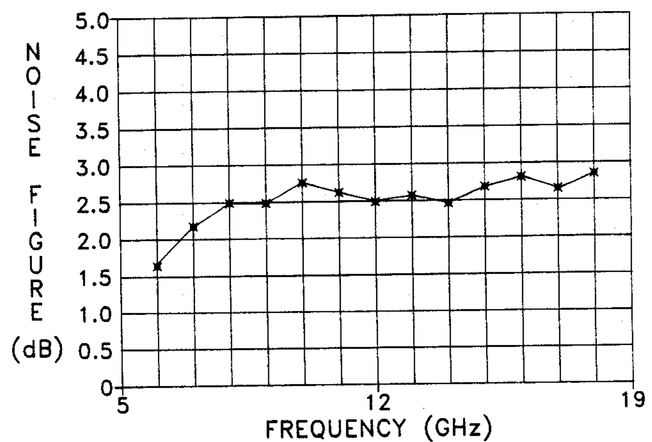

Figure 6C. On-carrier measured LNA noise figure.

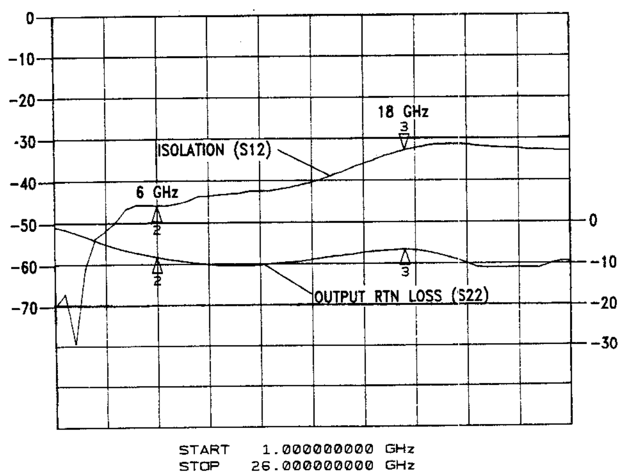

Figure 6B. On-wafer measured LNA reversed solation and output VSWR

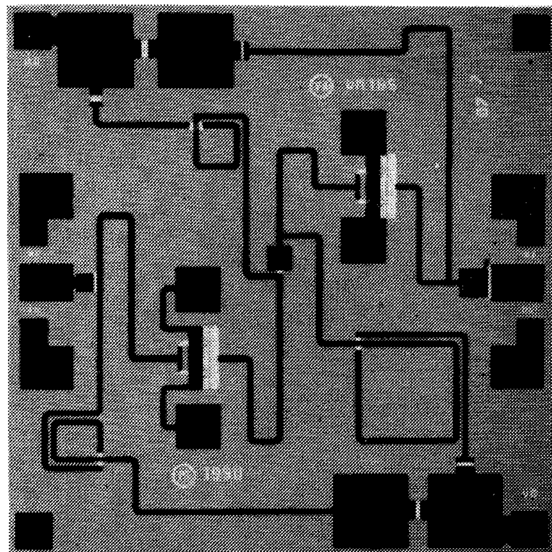

Figure 7. Photograph of the MMIC chip. Chip size is 0.064"x0.064"x0.004"

CONCLUSION

A high gain, very low noise figure, MMIC amplifier covering the 6 to 18 GHz band has been developed. This amplifier provides 15.0 dB gain, better than +/- 0.7 dB gain flatness, a 2.5 dB noise figure and +5dBm output power with a chip size of 0.064"x 0.064"x0.004". This MMIC device operates at a low DC power consumption. Its broadband performance, small size make it a good amplifier for EW applications.

ACKNOWLEDGMENT

The authors wish to thank C. Gamab, C. Manzon and J. Russell for their technical supports. This project was funded by Litton Solid State IR&D program.

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